R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR CLAIM AMENDMENTS

Support for the amendments to the claims can be found in the drawings as originally filed, for example, on FIGS. 1-5 and in the specification as originally filed, for example, on page 1, line 10 through page 2, line 13, on page 5, line 9 through page 6, line 14, on page 9, line 3 through page 10, line 8. As such, no new matter has been added.

OBJECTION TO THE SPECIFICATION

The objection to the specification under 35 U.S.C. §112, first paragraph, for failing to comply with the written description requirement to support the subject matter set forth in the claims is respectfully traversed and should be withdrawn.

The Office Action admits that the specification describes the delay times as providing "any appropriate delay in order to meet the criteria of a particular implementation (see page 3, lines 13-15 of the Office Action citing page 7, lines 10-11 of the specification). Clearly "any appropriate delay" would be understood as broad enough to include delays that can be described

as less than a period of the clock signal. The specification further states:

> For example, one of the delay elements 109a-109n may be appropriate to provide timing that may be used with a circuit such as the circuit 10 of FIG. 1. Furthermore, another one of the delay elements 109a-109n may provide a delay of the signal DLY appropriate with a circuit such as the circuit 20 of FIG. 2 (page 9, line 17 through page 10, line 1 of the specification).

The specification recites that the circuit 10 requires an aggressive data setup time and the circuit 20 requires an aggressive data hold time (see page 1, line 15 through page 2, line 10 of the specification. Thus, the specification clearly provides that the delay elements 109a-109n can provide delays on the order of an aggressive setup time and an aggressive hold time.

One skilled in the art would clearly be aware of the definition of the terms, "setup time" and "hold time" as evidenced by Fletcher, William I., An Engineering Approach to Digital Design, Prentice-Hall Inc., 1980, pages 320-323 (hereinafter Fletcher; attached as Exhibit A). In particular, one of ordinary skill in the art would understand that the setup time is the time required for the input data to settle in before the triggering edge of the clock signal (see definition of set-up time in section 5-20 on page 323 of Fletcher). Furthermore, one of ordinary skill in the art would understand that the definition of hold time is the time required for the data to remain stable after the triggering edge of

the clock signal (see definition of hold time in section 5-20 on page 323 of Fletcher). These definitions are consistent with the use of the terms in the specification (see page 1, lines 10-14 of the specification.

Furthermore, one of ordinary skill in the art would understand that the setup time and the hold time involve delay times that are less than the period of the clock (see FIGS. 5-38 and 5-41 in Fletcher). Furthermore, one of ordinary skill in the art would understand that a setup time or hold time greater than a period of the clock would not be reasonable since setup and hold time are defined with respect to a transition of the clock signal immediately following the setup time and immediately preceding the hold time.

Because setup time and hold time are defined with respect to a triggering edge of the clock signal and are understood to be less than a period of the clock signal, one or ordinary skill in the art would understand based on the description in the specification that the delay times referred to in the specification could be less than the period of the clock signal. As such, the disclosure of the application as originally filed, reasonably conveys to the artisan that the inventor had possession at the time of the presently claimed subject matter. *Vas Cath, Inc. v. Mahurkar*, 935 F. 2d. 1555, 1565, 19 USPQ2d. 1111, 1118 (Fed. Cir. 1991), *reh'rg denied* (Fed. Cir. July 8, 1991) and *reh'rg, en banc,*

denied (Fed. Cir. July 29, 1991). As such, the specification complies with the written description requirement under 35 U.S.C. §112, first paragraph, and the rejection should be withdrawn.

Furthermore, a patent need not teach, and preferably omits, what is well known in the art (MPEP §2164.01). The art of record may provide evidence of the level of knowledge of one of ordinary skill in the relevant art. The Office Action asserts that the art of record (i.e. Table 2 of Dallas Semiconductor Datasheet, "DS1020 Programmable 8-bit Silicon Delay Line," November 17, 1999) shows each of the plurality of delay times is less than a period of the clock signal. Thus, one of ordinary skill in the art would know of delay times that are less than a clock period. Therefore, the disclosures in the specification in the light of information known in the art would reasonably convey to the skilled artisan that the inventor had possession at the time of the invention of the claimed subject matter. As such, the specification complies with the written description requirement under 35 U.S.C. §112, first paragraph, and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §112, FIRST PARAGRAPH

The rejection of claims 1-13 and 15-21 under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one of skill in the relevant art that the inventor, at

the time of the application was filed, had possession of the claimed invention is respectfully traversed and should be withdrawn.

The Office Action admits that the specification describes the delay times as providing "any appropriate delay in order to meet the criteria of a particular implementation (see page 3, lines 13-15 of the Office Action citing page 7, lines 10-11 of the specification). Clearly "any appropriate delay" would be understood as broad enough to include delays that can be described as less than a period of the clock signal. The specification further states:

> For example, one of the delay elements 109a-109n may be appropriate to provide timing that may be used with a circuit such as the circuit 10 of FIG. 1. Furthermore, another one of the delay elements 109a-109n may provide a delay of the signal DLY appropriate with a circuit such as the circuit 20 of FIG. 2 (page 9,line 17 through page 10, line 1 of the specification).

The specification recites that the circuit 10 requires an aggressive data setup time and the circuit 20 requires an aggressive data hold time (see page 1, line 15 through page 2, line 10 of the specification. Thus, the specification clearly provides that the delay elements 109a-109n can provide delays on the order of an aggressive setup time and an aggressive hold time.

One skilled in the art would clearly be aware of the definition of the terms, "setup time" and "hold time" as evidenced

by Fletcher, William I., An Engineering Approach to Digital Design, Prentice-Hall Inc., 1980, pages 320-323 (hereinafter Fletcher; attached as Exhibit A). In particular, one of ordinary skill in the art would understand that the setup time is the time required for the input data to settle in before the triggering edge of the clock signal (see definition of set-up time in section 5-20 on page 323 of Fletcher). Furthermore, one of ordinary skill in the art would understand that the definition of hold time is the time required for the data to remain stable after the triggering edge of the clock signal (see definition of hold time in section 5-20 on page 323 of Fletcher). These definitions are consistent with the use of the terms in the specification (see page 1, lines 10-14 of the specification.

Furthermore, one of ordinary skill in the art would understand that the setup time and the hold time involve delay times that are less than the period of the clock (see FIGS. 5-38 and 5-41 in Fletcher). Furthermore, one of ordinary skill in the art would understand that a setup time or hold time greater than a period of the clock would not be reasonable since setup and hold time are defined with respect to a transition of the clock signal immediately following the setup time and immediately preceding the hold time.

Because setup time and hold time are defined with respect to a triggering edge of the clock signal and are understood to be

less than a period of the clock signal, one or ordinary skill in the art would understand based on the description in the specification that the delay times referred to in the specification could be less than the period of the clock signal. As such, the disclosure of the application as originally filed, reasonably conveys to the artisan that the inventor had possession at the time of the presently claimed subject matter. *Vas Cath, Inc. v. Mahurkar*, 935 F. 2d. 1555, 1565, 19 USPQ2d. 1111, 1118 (Fed. Cir. 1991), *reh'rg denied* (Fed. Cir. July 8, 1991) and *reh'rg, en banc, denied* (Fed. Cir. July 29, 1991). As such, claims 1-13 and 15-21 are fully patentable under 35 U.S.C. §112, first paragraph and the rejection should be withdrawn.

Furthermore, a patent need not teach, and preferably omits, what is well known in the art (MPEP §2164.01). The art of record may provide evidence of the level of knowledge of one of ordinary skill in the relevant art. The Office Action asserts that the art of record (i.e. Table 2 of Dallas Semiconductor Datasheet, "DS1020 Programmable 8-bit Silicon Delay Line," November 17, 1999) shows each of the plurality of delay times is less than a period of the clock signal. Thus, one of ordinary skill in the art would know of delay times that are less than a clock period. Therefore, the disclosures in the specification in the light of information known in the art would reasonably convey to the skilled artisan that the inventor had possession at the time of the invention of

the claimed subject matter. As such, claims 1-13 and 15-21 are fully patentable under 35 U.S.C. §112, first paragraph and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §112, SECOND PARAGRAPH

The rejection of claims 12 and 18-20 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention has been obviated by appropriate amendment and should be withdrawn.

The rejection of claim 21 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention is respectfully traversed and should be withdrawn. Applicants' representative disagrees with the characterization of claim 21 as being a substantial duplicate of claim 1 (See page 4, lines 5-9 of the Office Action.) 37 CFR §1.75 provides that one or more claims may be presented in dependent form referring back to and further limiting another claim or claims in the same application (37 CFR §1.75(c)). Claim 21 further limits claim 1 and therefore, is a proper dependent claim under 37 CFR §1.75.

Specifically, claim 1 provides a plurality of delay times where each of the plurality of delay times is less than a period of the clock signal. Claim 1 does not limit the total of the

plurality of delay times to a period of time less than the period of the clock signal. In contrast, claim 21 provides the further limitation that a total of all of the plurality of delay times is less than the period of the clock signal. Therefore, claim 21 further limits claim 1 and is a proper dependent claim under 37 CFR §1.75(c). As such, the objection to claim 21 should be withdrawn.

As such, claims 12 and 18-21 are fully patentable under 35 U.S.C. §112, second paragraph and the rejections should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1-3, 11-13 and 15-21 under 35 U.S.C. §103(a) as being unpatentable over Conn et al. (U.S. Patent No. 6, 150,863, hereinafter Conn) in view of Dallas Semiconductor Datasheet, "DS1020 Programmable 8-bit Silicon Delay Line," November 17, 1999 (hereinafter Dallas) has been obviated by appropriate amendment and should be withdrawn.

The rejection of claim 4 and 5-10 under 35 U.S.C. §103(a) as being unpatentable over Conn in view of Dallas and in further view of JEDEC Standard No. 8-6, "High Speed Transceiver Logic (HSTL) - A 1.5 V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits," EIA/JESD8-6, August 1995 (hereinafter JEDEC) has been obviated by appropriate amendment and should be withdrawn.

Conn is directed to a user controlled delay circuit for a programmable logic device (Title). Dallas disclose a programmable 8-bit silicon delay line (Title). Conn and Dallas, alone or in combination, do not teach or suggest each and every element of the presently claimed invention. Specifically, assuming *arguendo*, (i) the clock pad 505 of Conn is similar to the presently claimed first input, (ii) the IO pad 220a of Conn is similar to the presently claimed second input, (iii) the circuit 210a of Conn is similar to the presently claimed first circuit and (iv) the circuit 510a of Conn is similar to the present claimed second circuit, Conn does not teach or suggest a second circuit configured to receive the delayed data signal from the first circuit and the clock signal **from the first input**, as presently claimed in claim 1. In particular, the clock CLK of Conn received by the circuit 510a of Conn comes from an output of the delay element 530 of Conn rather than from the clock pad 505. Therefore, Conn and Dallas do not teach or suggest each and every element of the presently pending claim 1. Claims 11 and 12 include similar limitations. As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Claims 4-10 and 21 each depend, either directly or indirectly, from claim 1, which is believed to be allowable. Claims 15-20 each depend, either directly or indirectly, from claim 12, which is believed to be allowable. As such, the presently

claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

New claims 22-23 depend directly from claim 1 which is believed to be allowable. As such, the presently claimed invention is fully patentable over the cited references.

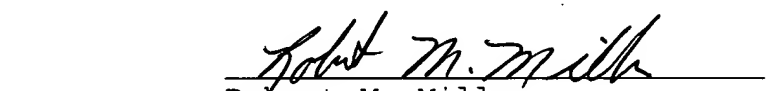
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



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